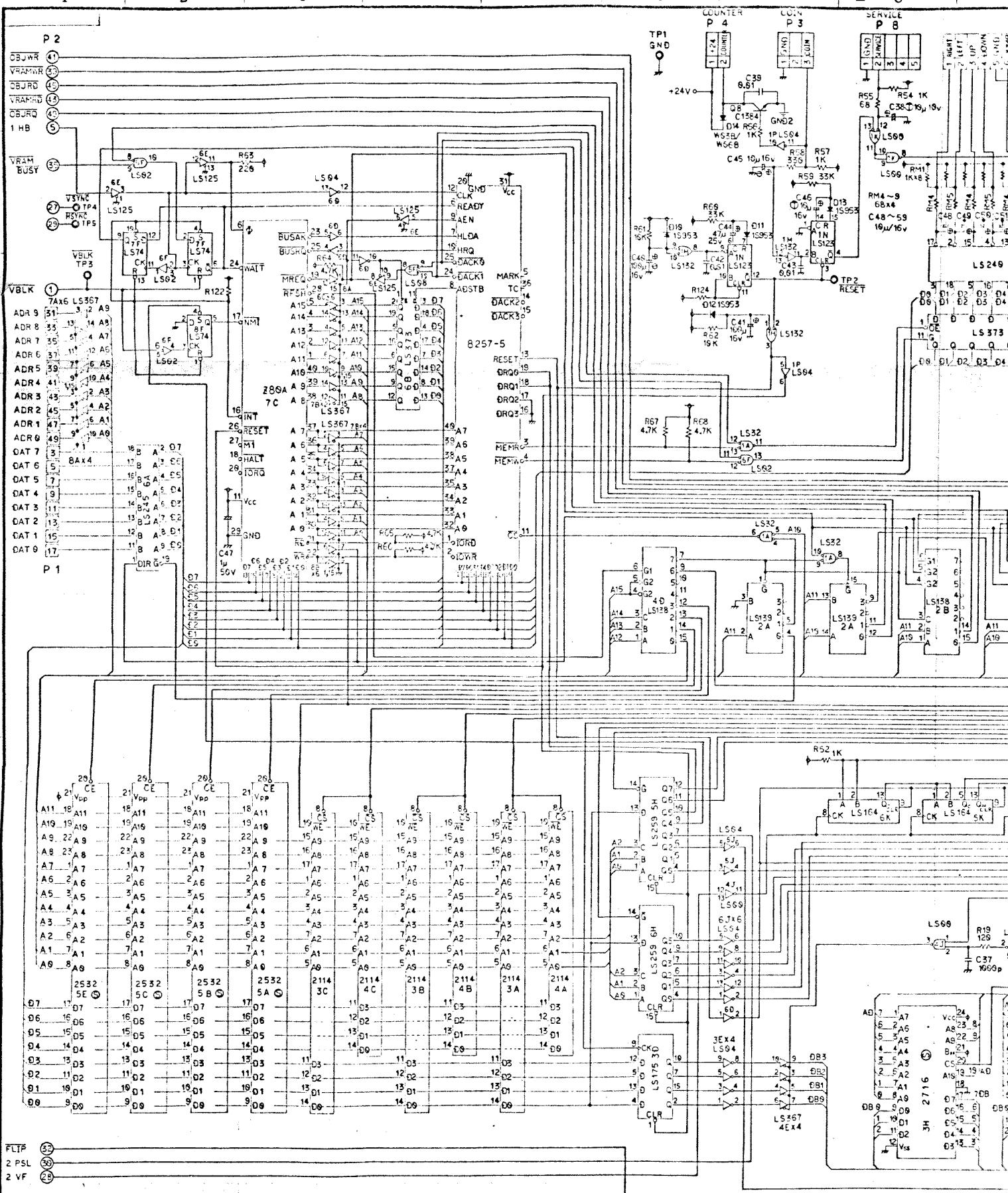


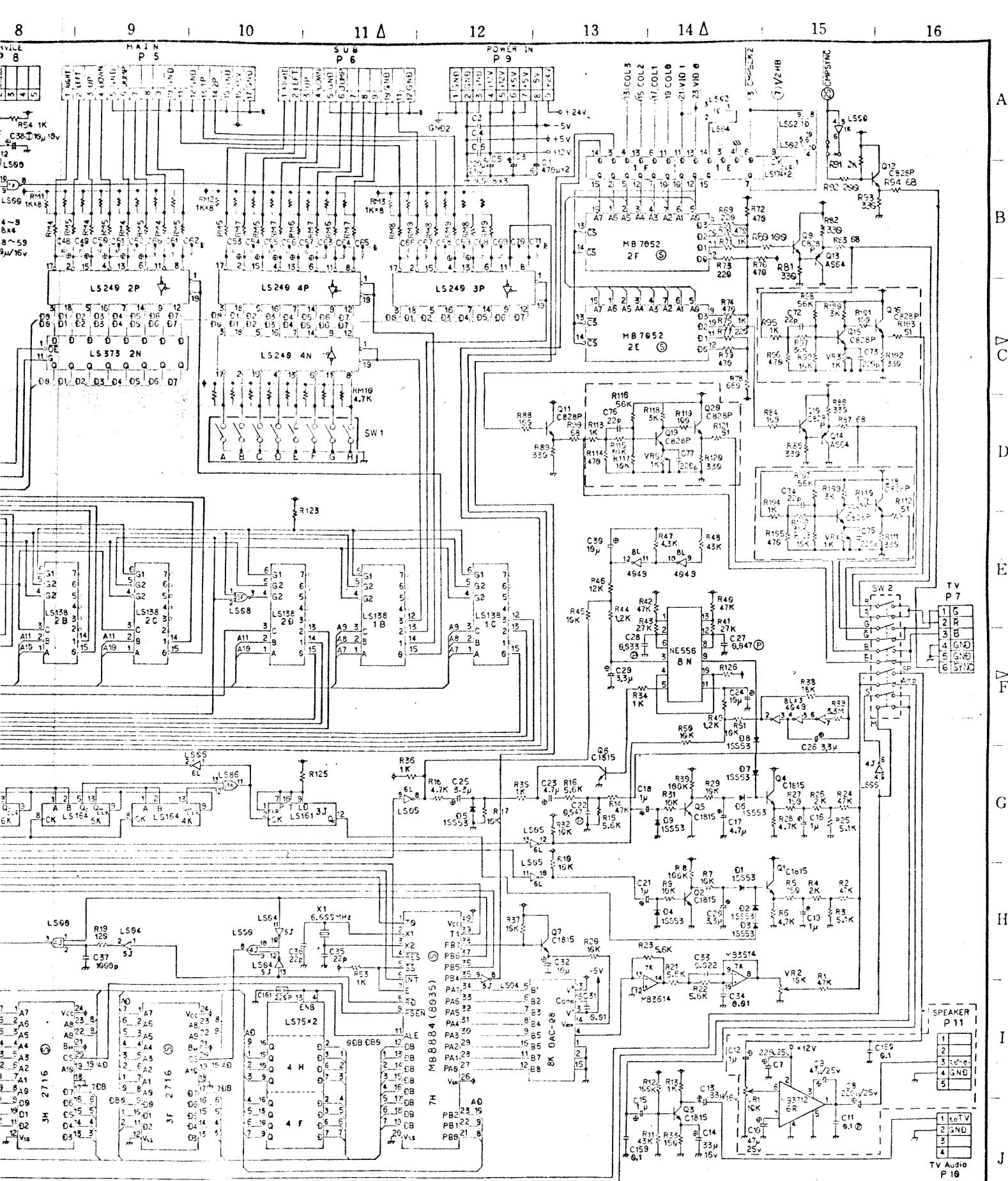
DONKEY KONG

SCHEMATICS

Nintendo

T K G - 4





Note 2 : - : OPTION PARTS

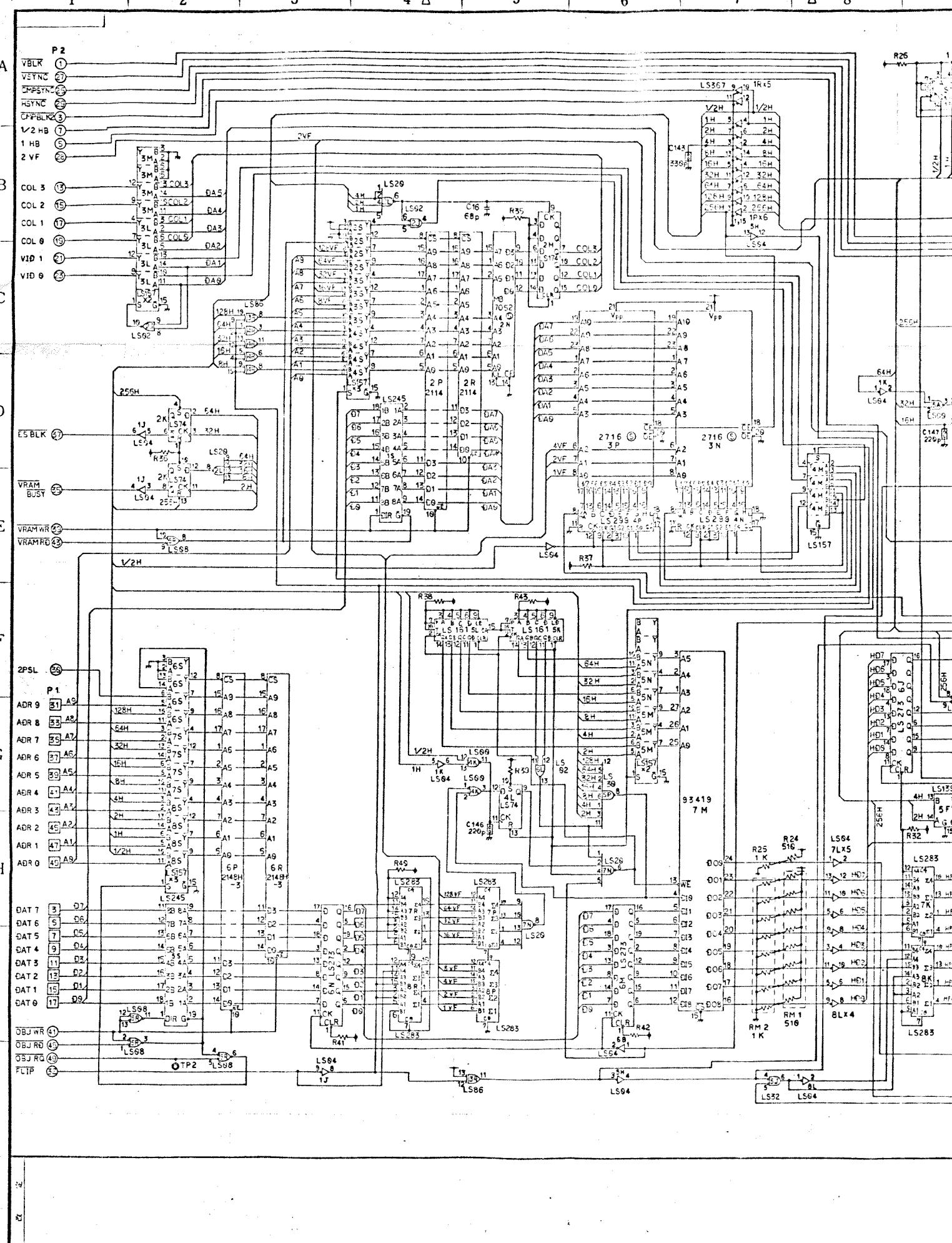
-5V	GND	+5V
2 3 4 5 6 7 8 9 0		

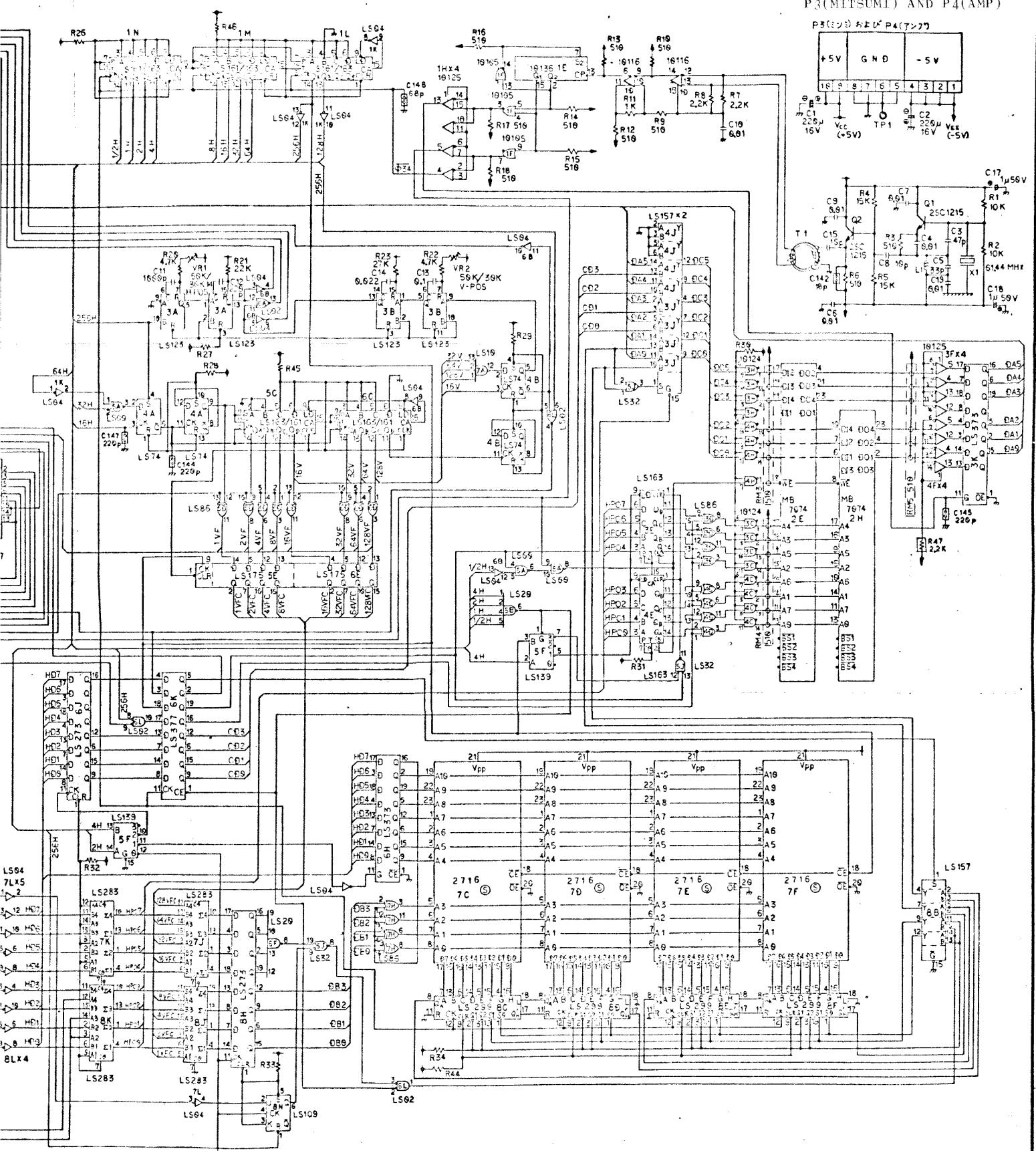
P1 P2 ARRANGE

TKG4-13-CPU

S.56.12.1

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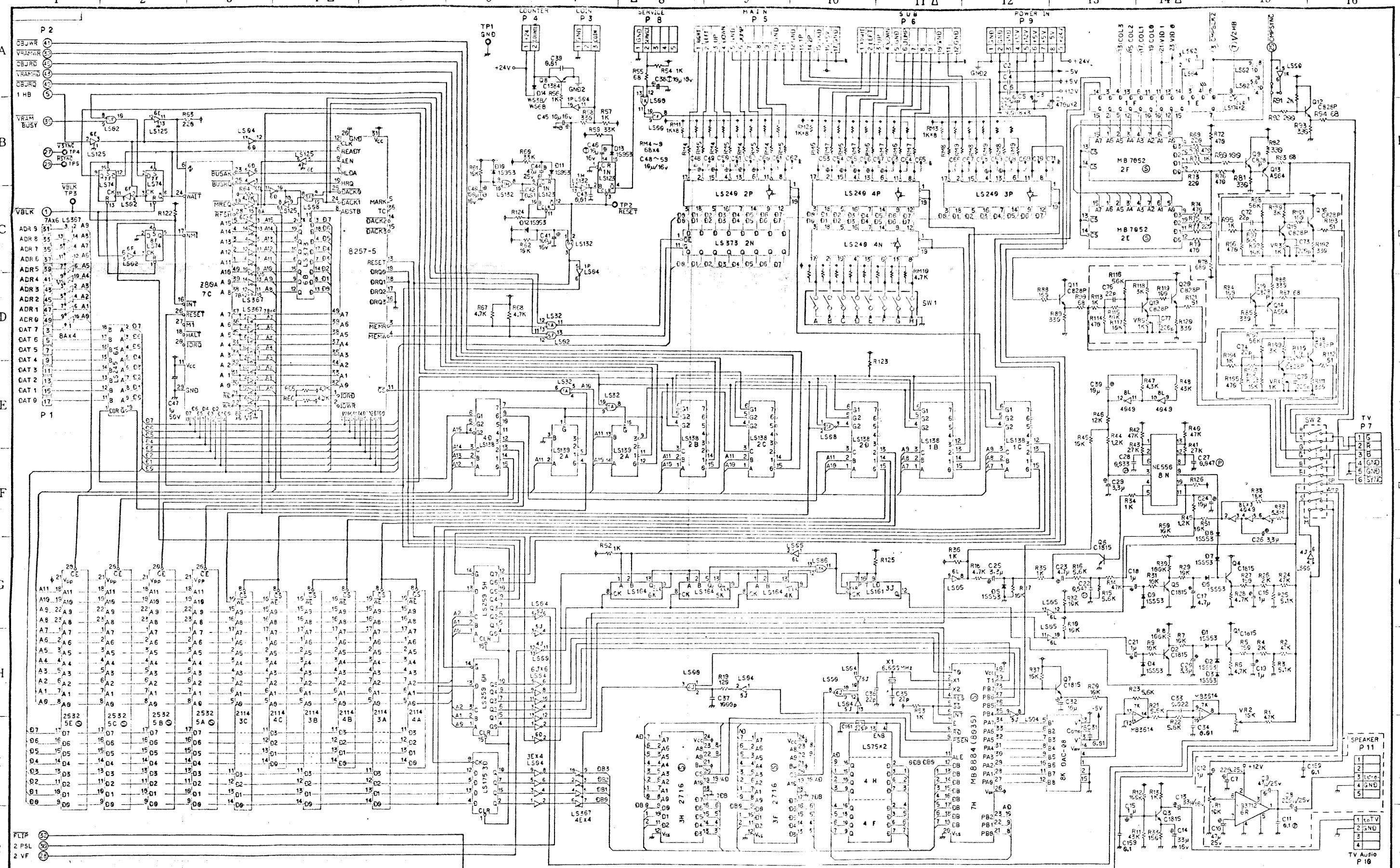




P3(MITSUMI) AND P4(AMP)

P3(ミンミ) および P4(アンフウ)

The diagram illustrates the internal circuit of the 741 operational amplifier. It features a central triangular core with three main stages: an input stage (NPN), a voltage-controlled voltage source (VCS) stage (NPN), and an output stage (NPN). The input stage consists of transistors Q1 and Q2. The VCS stage is controlled by the non-inverting input (pin 3) through transistor Q3. The output stage is driven by the VCS stage and includes transistors Q4 and Q5. The circuit is powered by ±15V supplies (V_{CC} and V_{EE}) and includes biasing resistors R_{B1} and R_{B2}, and feedback resistors R_{F1} and R_{F2}. The ground connection (GND) is at pin 4.



Note 1 EDGE-CONNECTOR (PIN ARRANGEMENT)

5	+1SV	
6	-5V	
7		2.PLAY
8		9.PLAY
9		10.PLAY
10		11.PLAY
11		12.PLAY
12		13.PLAY
13		14.PLAY
14		15.PLAY
15		16.PLAY
16		17.PLAY
17		18.PLAY
18		19.PLAY
19		20.PLAY
20		21.PLAY
21		22.PLAY
22		23.PLAY
23		24.PLAY
24		25.PLAY
25		26.PLAY
26		27.PLAY
27		28.PLAY
28		29.PLAY
29		30.PLAY
30		31.PLAY
31		32.PLAY
32		33.PLAY
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34		35.PLAY
35		36.PLAY
36		37.PLAY
37		38.PLAY
38		39.PLAY
39		40.PLAY
40		41.PLAY
41		42.PLAY
42		43.PLAY
43		44.PLAY
44		45.PLAY
45		46.PLAY
46		47.PLAY
47		48.PLAY
48		49.PLAY
49		50.PLAY
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67		68.PLAY
68		69.PLAY
69		70.PLAY
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465		466.PLAY
466		467.PLAY
467		468.PLAY
468		469.PLAY
469		470.PLAY
470		471.PLAY
471		472.PLAY
472		473.PLAY
473		474.PLAY
474		475.PLAY
475		476.PLAY
476		477.PLAY
477		478.PLAY
478		479.PLAY
479		480.PLAY

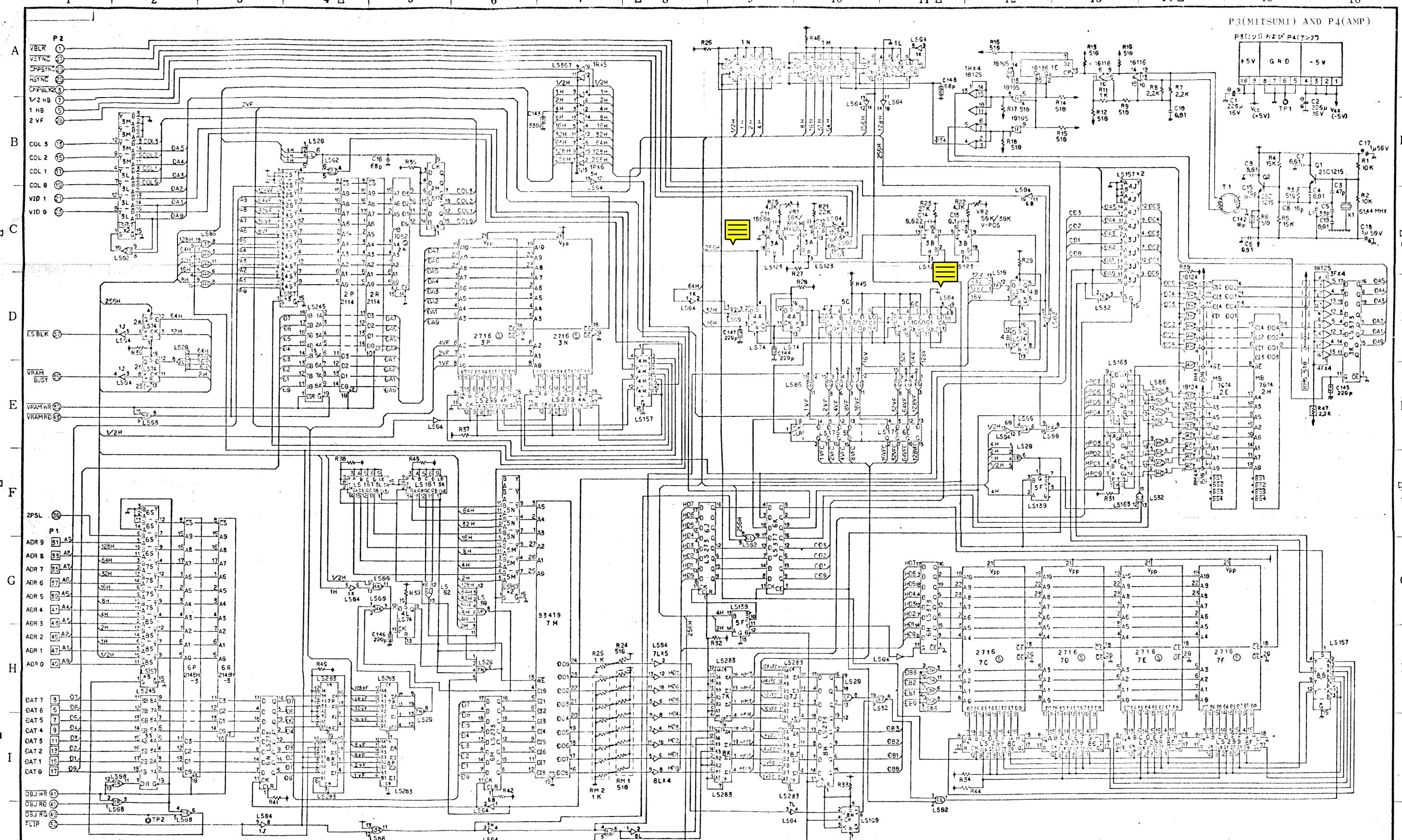
1P:MAIN SIDE
2P:SUB SIDE
1 PLAY:1 PLAYER SWITCH
2 PLAY:2 PLAYER SWITCH

Note 2 : OPTION PARTS

-5V	GND	+5V
1 2 3 4 5 6 7 8 9 10		

TKG4-13-CPU

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P 3(MITSUMI) AND P 4(AMP)

P3(ミンミ) および P4(アンフフ)

7674 7674
2 E 2 H
17 A4
16 A3
9 AS
15 A2
19 A6
14 A1
11 A7
13 A9
1 B51
2 B52
3 B53
4 B54

The diagram illustrates the internal logic and pin connections of a LS157 integrated circuit. The IC is shown in a dual-in-line package (DIP) with 20 pins. Pin 18 is labeled 'V_{PP}' and Pin 19 is labeled 'GND'. The internal logic is organized into several functional blocks:

- Left Column:** Contains a 716 flip-flop (labeled 716 with a circle symbol). Its outputs are connected to the clock inputs of two 4-to-1 multiplexers (labeled 140).
- Middle Column:** Contains a 4-to-1 multiplexer (labeled 140), followed by a 4-to-1 decoder (labeled 141).
- Right Column:** Contains a 4-to-1 decoder (labeled 141), followed by a 4-to-1 multiplexer (labeled 140).
- Bottom Row:** Contains a 4-to-1 multiplexer (labeled 140), followed by a 4-to-1 decoder (labeled 141).
- Top Row:** Contains a 4-to-1 decoder (labeled 141), followed by a 4-to-1 multiplexer (labeled 140).
- Bottom Left:** Contains a 4-to-1 multiplexer (labeled 140).
- Bottom Right:** Contains a 4-to-1 decoder (labeled 141).

Interconnections between these blocks are indicated by lines connecting their respective output and input pins.

品名	任天堂	数量	单数
KG4-13-VIDEO		販売年月	S.56.12.1
任天堂株式会社		単位	箱
Nintendo Co., Ltd.		角法	